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AN ALGORITHM FOR FLOORPLANNING, PLACEMENT AND ROUTING THROUGH SILICON VIAS IN 3D VLSI

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Abstract

Dominance of on-chip power densities has become a critical design constraint in high-performance VLSI design. This is primarily due to increased technology scaling, number of components, frequency and bandwidth. The consumed power is usually converted into dissipated heat, affecting the performance and reliability of a chip. Moreover, recent trends in VLSI design entail the stacking of multiple active (device) layers into a monolithic chip. These 3D chips have significantly larger power densities than their 2D counterparts. In this project, we consider the thermal placement of standard cells and gate arrays (modules) taking total wire-length as well as TSVs (through silicon via) into consideration. Our contribution includes a novel algorithm for placement of the gates or cell in the different active layers of a 3D IC such that: (i) the temperatures of the modules in each of the active layers is uniformly distributed, (ii) the maximum temperatures of the active layers are not too high, (iii) the maximum temperatures of the layers vary in a non-increasing manner from bottom layer to top layer, (iv) the estimated total interconnect lengths connecting the modules of the different layers are also improved, and (v) the total number of interlayer vias is quite reasonable. Experimental results on randomly generated and standard benchmark instances are encouraging. Therefore, in this project, we have studied and proposed a two-stage 3-D fixed-outline floorplanning algorithm using TSVs. Stage one develops a floorplan for thermal disparity minimization and the Stage two improves the wirelength by assigning signal TSVs. Experimental results show that compared to the post-processing TSV planning algorithm, i.e. the average wirelength for the floorplan developed by stage one of our result is reduced by around 45.3% using the stage two.

Keywords: Placement, Netlist, Thermal Aware, TSVs, Blocks, Pin_connectivity.